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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,917	07/23/2003	Shahram Mostafazadeh	NSC1P194D1/P04836D1	9491

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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/625,917	MOSTAFAZADEH, SHAHRAM	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the after final amendment filed 18 March 2005.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8,11-12 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al. (U.S. Patent 6,255,740) in view of Moden (U.S. Patent 5,719,440).

Tsuji discloses a semiconductor device (Fig. 21c) that contains a first die (41), a plurality of lead posts (28a) each of the lead posts positioned on a plurality of lead fingers (63) respectively, each of the plurality of lead fingers electrically isolated from the one another, an encapsulating material (23a/51a) encapsulating the first die, lead posts and formed between the plurality of lead fingers to electrically isolate the lead fingers from each other, the lead posts have equal spacing and pitch and have a square cross section or round cross section (Figs. 19b and 27b) and have lengths that are substantially perpendicular to the conductive side of the die and an oversized contact

pad (71) on the bottom surface of the integrated circuit outside the encapsulant and has a diameter larger than the diameter of the lead post. (Fig. 23) The die can be directly connected to the lead posts. (Fig. 40c) Tsuji discloses all the limitations except for the conductive side of the chip faces the plurality of lead posts. Whereas Moden discloses a chip package (Fig. 1) that contains a die (12) with a conductive side, plurality of lead posts (16) wherein the conductive side of the first die faces the plurality of lead posts and are mechanically and electrically connected to the lead posts with epoxy to a plurality of conductive pads (15). The conductive side of the die faces the plurality of lead posts and is connected to the lead posts by conductive pads to electrically connect the die to the lead posts. (Abstract) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Tsuji by incorporating the conductive side of the die to face the plurality of lead posts to electrically connect the die to the lead posts as taught by Moden.

Claims 9,10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji and Moden in view of Wang (U.S. Patent 6,258,626).

Tsuji and Moden disclose all the limitations except for a second die connected to the first die. Whereas Wang discloses a semiconductor package (Fig. 1) that contains a first die (110) with a conductive side, a second die (130) with a conductive side and a side opposite the conductive side of the first die wherein the side opposite the conductive side connected to a side opposite the conductive side of the first die, lead posts (112/124) a wirebonding (132) connected between the conductive side of the second die and at least one of the lead posts, and encapsulate (140) encapsulating the

first and second die, lead post and wirebonding. A second die is connected to the first die for flip chip connection. (Column 1, lines 12-14) Therefore it would be obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Tsuji and Moden by incorporating a second die connected to the first die for flip chip connection as taught by Wang.

Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (U.S. Patent 5,830,800) in view of Moden.

Lin discloses a ball grid array (Figs. 1d-f) that contains a lead frame (10) having a first surface and a substantially planar second surface, a set of posts (30) formed on the first surface of the lead frame, the plurality of post organized into a plurality of subsets of posts, a plurality of semiconductor die (40) each mounted onto the plurality of subsets of posts with epoxy to the conductive pads and an encapsulant (50) encapsulating the lead frame including plurality of semiconductor die and subsets of posts, the substantially planar second surface of the lead frame acting to prevent the encapsulate from forming on the second surface of the lead frame where a space is formed between the plurality of die for singulate the individual semiconductor die from the lead frame using a cutting tool. In reference to the encapsulation being continuous that is an intermediate process since the final process is singulating the lead frame which makes each die individually encapsulated and the Lin reference would be continuously encapsulated. Therefore that limitation is not distinguishable over the art because it is an intermediate process not the final product, which is separate dies. Lin discloses all the limitations except for the conductive side of the chip faces the plurality of lead posts.

Whereas Moden discloses a chip package (Fig. 1) that contains a die (12) with a conductive side, plurality of lead posts (16) wherein the conductive side of the first die faces the plurality of lead posts and are mechanically and electrically connected to the lead posts with epoxy to a plurality of conductive pads (15). The conductive side of the die faces the plurality of lead posts and is connected to the lead posts by conductive pads to electrically connect the die to the lead posts. (Abstract) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Lin by incorporating the conductive side of the die to face the plurality of lead posts to electrically connect the die to the lead posts as taught by Moden.

Response to Arguments

Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR

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